WE CLAIM:

1. A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer; and

depositing a dielectric layer over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species; and

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material.

2. The method of Claim 1, wherein the textured silicon layer comprises a hemispherical grain morphology.

3. The method of Claim 1, wherein forming no more than about one monolayer comprises supplying a first chemistry substantially excluding the second reactant species and reacting comprises supplying a second chemistry substantially excluding the first reactant species.

4. The method of Claim 3, further comprising repeatedly alternating supplying the first chemistry and supplying the second chemistry until a dielectric layer forms having a thickness between about 10 Å and 200 Å.

5. The method of Claim 4, further comprising supplying a carrier gas while repeatedly alternating supplying the first chemistry and supplying the second chemistry.

6. The method of Claim 5, wherein the carrier gas purges reactants between supplying the first chemistry and supplying the second chemistry.

7. The method of Claim 6, wherein supplying the first chemistry is stopped and the reaction chamber is purged with more than about two chamber volumes of purge gas before supplying the second chemistry.

8. The method of Claim 1, wherein depositing the dielectric layer further comprises exposing the second material to a third reactant species to leave no more than about one monolayer of a third material.

9. The method of Claim 8, wherein the dielectric layer comprises two different metals and oxygen.

9/10. The method of Claim 8/9, wherein the dielectric layer comprises a metal, silicon and oxygen.

10/11. The method of Claim 1, wherein the dielectric layer has a dielectric constant of greater than about 10.

11/12. The method of Claim 10/11, wherein the dielectric layer is selected from the group consisting of aluminum oxide, tantalum oxide, titanium oxide, zirconium oxide, niobium oxide, hafnium oxide, silicon oxide and mixtures and compounds thereof.

12/13. The method of Claim 10/11, wherein the dielectric layer has a dielectric constant equal to or greater than about 20.

13/14. The method of Claim 1, wherein the first material is self-terminated.

14/15. The method of Claim 13/14, wherein the first material is terminated by halide ligands.

15/16. The method of Claim 14/15, wherein the first reactant species comprises a zirconium halide and the second reactant species comprises an oxygen-containing source gas.

16/17. The method of Claim 17/14, wherein the first material is terminated by organic ligands.

17/18. The method of Claim 1, wherein the first material comprises methyl-terminated aluminum and the second reactant species comprises an oxygen-containing source gas.

18/19. The method of Claim 1, wherein the first material comprises ethoxide-terminated tantalum and the second reactant species comprises an oxygen-containing source gas.

19/20. The method of Claim 1, further comprising forming a barrier layer directly on the textured silicon surface prior to forming no more than about one monolayer.

20/21. The method of Claim 19/20, wherein forming a barrier layer comprises nitriding the textured silicon surface.

21/22. The method of Claim 19/20, wherein forming a barrier layer comprises oxidizing the textured silicon surface to form a silicon oxide and nitriding the silicon oxide.

22 ~~23~~. The method of Claim 1, wherein bottom electrode conforms to a three-dimensional folding structure.

23 ~~24~~. The method of Claim 22, wherein the bottom electrode conforms to a trench within a semiconductor substrate.

24 ~~25~~. The method of Claim 22, wherein the three-dimensional folding shape is formed above a semiconductor substrate.

25 ~~26~~. The method of Claim 24, wherein the three-dimensional shape defines an interior volume.

26 ~~27~~. The method of Claim 25, wherein the three-dimensional shape conforms to a cylinder.

27 ~~28~~. The method of Claim 1, further comprising depositing a conductive layer over the dielectric layer, wherein depositing the conductive layer comprises:

forming no more than about one monolayer of a third material over the dielectric layer by exposure to a third reactant species; and

reacting a fourth reactant species with the third material to leave no more than about one monolayer of a fourth material.

28 ~~29~~. The method of Claim 27, wherein the third reactant species comprises a metal complex, the fourth reactant species comprises a nitrogen-containing source gas, and the conductive layer comprises a metal nitride.

30. A method of forming a dielectric layer having a dielectric constant greater than about 10 over a textured bottom electrode in an integrated circuit, comprising:

forming no more than about one monolayer of a metal-containing species in a self-limited reaction; and

reacting an oxygen-containing species with the monolayer.

31. The method of Claim 30, wherein the textured bottom electrode comprises silicon.

32. The method of Claim 31, wherein the textured bottom electrode has a hemispherical grain morphology.

29 ~~30~~ ~~31~~. The method of Claim 30, wherein the self-limited reaction comprises forming a halogen-terminated metal film.

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~~34~~. The method of Claim ~~33~~, wherein reacting the oxygen-containing species comprises a ligand-exchange reaction.

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~~35~~. The method of Claim ~~30~~, further comprising repeating forming no more than about one monolayer and reacting the oxygen-containing species at least about 10 times until the dielectric layer has a desired thickness.

36. A capacitor structure in an integrated circuit, comprising;

a bottom electrode conforming to a macrostructural three-dimensional folding shape and a having a textured silicon surface;

a capacitor dielectric having a dielectric constant greater than about 10 conforming to the textured surface, the dielectric having a maximum thickness of less than about 100 Å and a minimum thickness greater than about 95% of the maximum thickness.

37. The structure of Claim 36, further comprising a top electrode conforming to the dielectric, the top electrode continuously contacting the dielectric over the entire textured surface.

38. The structure of Claim 37, wherein the top electrode comprises a conductive barrier layer continuously contacting the dielectric over the entire textured surface and a more conductive material formed over the conductive barrier layer.

39. The structure of Claim 37, wherein the top electrode comprises an elemental metal layer continuously contacting the dielectric over the entire textured surface.

40. The structure of Claim 36, wherein the capacitor dielectric comprises a metal oxide.

41. The structure of Claim 40, wherein the metal oxide comprises aluminum oxide.

42. The structure of Claim 40, wherein the metal oxide comprises an oxide of a transition metal.

43. The structure of Claim 42, further comprising a conformal barrier layer formed between the textured silicon layer and the dielectric.

44. The structure of Claim 42, wherein the metal oxide layer comprises an oxide of a Group IV transition metal.

55. A process of forming a capacitor dielectric over a hemispherical grain silicon surface, comprising:

coating the hemispherical grain silicon surface with no more than about one monolayer of a ligand-terminated metal complex in a first phase;

replacing ligands of the ligand-terminated metal with oxygen in a second phase distinct from the first phase; and

repeating the first and second phases in at least about 10 cycles.

34 ~~56~~. The process of Claim ~~55~~ 33, wherein each cycle comprises a third phase, the third phase comprising adsorbing no more than about one monolayer of a second ligand-terminated metal after the second phase.

35 ~~57~~. The process of Claim ~~56~~ 34, wherein each cycle further comprises a fourth phase, the fourth phase comprising replacing ligands of the second ligand-terminated metal with oxygen.

36 ~~58~~. The process of Claim ~~57~~ 35, wherein the first phase comprises pulsing a first oxygen-containing species.

37 ~~59~~. The process of Claim ~~58~~ 36, wherein the fourth phase comprises pulsing a different oxygen-containing species.

38 ~~60~~. The process of Claim ~~55~~ 33, wherein the ligand-terminated metal comprises a metal ethoxide complex.

39 ~~61~~. The process of Claim ~~55~~ 33, wherein the ligand-terminated metal comprises a metal chloride complex.

40 ~~62~~. The process of Claim ~~55~~ 37, comprising maintaining a temperature of less than about 350°C.

63. A method of forming a capacitor with high surface area in an integrated circuit, comprising:

forming a bottom electrode in a three-dimensional folding shape;

superimposing a textured morphology over the three-dimensional folding shape; and

depositing a layer conformally over the textured morphology by cyclically supplying at least two alternating, self-terminating chemistries, the layer forming part of the capacitor .

45. The structure of Claim 42, wherein the metal oxide comprises an oxide of a Group V transition metal.

46. The structure of Claim 36, wherein the dielectric comprises a ternary material.

47. The structure of Claim 46, wherein the dielectric comprises a metal, silicon and oxygen.

48. The structure of Claim 36, wherein the dielectric has a thickness between about 25 Å and 100 Å.

49. The structure of Claim 36, wherein the minimum thickness is at least about 98% of the maximum thickness.

50. An integrated circuit having a plurality of memory cells, each memory cell including a capacitor comprising:

a first electrode having a surface conforming to a hemispherical grain morphology;

a capacitor dielectric layer adjacent to the first electrode and conforming to the hemispherical grain morphology, the capacitor dielectric comprising a material selected from the group consisting of aluminum oxide, titanium oxide, zirconium oxide, niobium oxide, hafnium oxide, silicon oxide and mixtures and compounds thereof; and

a second electrode adjacent to and conforming to the hemispherical grain morphology.

51. The integrated circuit of Claim 50, wherein the capacitor dielectric layer has a thickness between about 10 Å and 200 Å.

52. The integrated circuit of Claim 50, wherein the capacitor dielectric layer has a maximum thickness over the first electrode and a minimum thickness over the first electrode no more than about 95% of the maximum thickness.

53. The integrated circuit of Claim 50, wherein the capacitor dielectric layer further comprises a plurality of sublayers.

54. The integrated circuit of Claim 53, wherein the sublayers comprise a plurality of sublayers of afirst metal oxide alternated with the sublayers of an other metal oxide.

64. The method of Claim 63, wherein the layer comprises a capacitor dielectric in direct contact with the bottom electrode.

65. The method of Claim 63, wherein the layer comprises a thin conductive layer overlying a capacitor dielectric, where the capacitor dielectric directly contacts the bottom electrode.

66. The method of Claim 65, wherein the bottom electrode comprises a hemispherical grain silicon layer.